WHAT IS CLAIMED IS:

1. A logic circuit optimizing method, comprising:

clustering logic circuits included in inputted logic circuit information to obtain primary clusters;

inserting a flip-flop to a cluster whose cluster length exceeds predetermined cluster length, the cluster being one of the primary clusters obtained in said clustering; and

re-clustering the flip-flop inserted cluster to obtain secondary clusters.

2. The logic circuit optimizing method as defined in claim 1, wherein said inserting a flip-flop to a cluster comprises:

measuring cluster length of each of the primary clusters obtained in said clustering;

selecting a cluster whose cluster length exceeds the predetermined cluster length, the cluster being one of the primary clusters obtained in said clustering; and

inserting a flip-flop to the selected cluster,

wherein, when there exists a cluster whose cluster length exceeds the predetermined cluster length among the primary clusters obtained in said clustering, said inserting a flip-flop to the selected cluster and said re-clustering the flip-flop inserted cluster are performed.

3. The logic circuit optimizing method as defined in claim 1, further comprising:

inserting a flip-flop to a cluster that is too large to be contained in a variable logic element of a logic emulation device, when the cluster is allotted to the variable logic element, the cluster being included in logic circuit information after said clustering and said re-clustering; and

re-clustering the flip-flop inserted cluster.

4. The logic circuit optimizing method as defined in claim 1, further

comprising: substituting a logic circuit for a to-be-logically-emulated memory device, by expressing a memory device in terms of circuit length, the memory device embodying the to-be-logically-emulated memory device.

5. The logic circuit optimizing method as defined in claim 4, wherein the circuit length is expressed in terms of a number of cascading circuit stages.

6. The logic circuit optimizing method as defined in claim 4, wherein the circuit length is expressed in terms of a signal propagation time.

7. The logic circuit optimizing method as defined in claim 1, wherein the cluster length is expressed in terms of a number of cascading circuit stages.

8. The logic circuit optimizing method as defined in claim 1, wherein the cluster length is expressed in terms of a signal propagation time.

9. A logic circuit optimizing method, comprising:

inserting a flip-flop to a cluster that is too large to be contained in a variable logic element of a logic emulation device, when the cluster is allotted to the variable logic element, the cluster being included in logic circuit information after clustering; and

re-clustering the flip-flop inserted cluster.

10. The logic circuit optimizing method as defined in claim 1, wherein an operation clock frequency of a new flip-flop to be inserted is higher than that of a flip-flop already included in a cluster to which the new flip-flop is to be inserted.

11. A logic circuit optimizing method, comprising:

calculating a number of operational elements included in a module that is described by hardware description language; and

inserting a flip-flop described by hardware description language to a module that possesses operational elements more than a prescribed number.

12. A logic circuit optimizing device, comprising:

a clustering unit operable to cluster logic circuits included in inputted logic

circuit information to obtain primary clusters;

a circuit dividing unit operable to insert a flip-flop to a cluster whose cluster length exceeds predetermined cluster length, the cluster being one of the primary clusters obtained by said clustering unit,

wherein said clustering unit re-clusters the flip-flop inserted cluster to obtain secondary clusters.

13. The logic circuit optimizing device as defined in claim 12, further comprising:

a cluster length measuring unit operable to measure cluster length of each of the primary clusters obtained by said clustering unit; and

a selecting unit operable to select a cluster whose cluster length exceeds the predetermined cluster length, the cluster being one of the primary clusters obtained by said clustering unit;

wherein, when there exists a cluster whose cluster length exceeds the predetermined cluster length among the primary clusters obtained by said clustering unit, said circuit dividing unit inserts a flip-flop to the cluster whose cluster length exceeds the predetermined cluster length.

14. The logic circuit optimizing device as defined in claim 12, wherein,

said circuit dividing unit inserts a flip-flop to a cluster that is too large to be contained in a variable logic element of a logic emulation device, when the cluster is allotted to the variable logic element, the cluster being included in logic circuit information after the clustering and re-clustering; and

said clustering unit re-clusters the flip-flop inserted cluster.

15. The logic circuit optimizing device as defined in claim 12, further comprising a substitution unit operable to substitute a logic circuit for a to-be-logically-emulated memory device, by expressing a memory device in terms of circuit length, the memory device embodying the to-be-logically-emulated memory

device.

16. The logic circuit optimizing device as defined in claim 15, wherein the circuit length is expressed in terms of a number of cascading circuit stages.

17. The logic circuit optimizing device as defined in claim 15, wherein the circuit length is expressed in terms of a signal propagation time.

18. The logic circuit optimizing device as defined in claim 12, wherein the cluster length is expressed in terms of a number of cascading circuit stages.

19. The logic circuit optimizing device as defined in claim 12, wherein the cluster length is expressed in terms of a signal propagation time.

20. A logic circuit optimizing device, comprising:

a circuit dividing unit operable to insert a flip-flop to a cluster that is too large to be contained in a variable logic element of a logic emulation device, when the cluster is allotted to the variable logic element, the cluster being included in logic circuit information after clustering; and

a clustering unit operable to re-cluster the flip-flop inserted cluster.

21. The logic circuit optimizing device as defined in claim 12, wherein an operation clock frequency of a new flip-flop to be inserted is higher than that of a flip-flop already included in a cluster to which the new flip-flop is to be inserted.

22. A logic circuit composing device, comprising:

an operational-element-number calculating unit operable to calculate a number of operational elements included in a module that is described by hardware description language; and

a module dividing unit operable to insert a flip-flop described by hardware description language to a module that possesses operational elements more than a prescribed number.